# Self-Aligned Mask to Reduce Cell Layout Area

## TECHNICAL FIELD

**[0001]** The present invention relates to the manufacture of semiconductor devices and more particularly to a method of reducing the area of a semiconductor cell by using a self-aligned mask for etching selected features, such as a via or trench, from an upper level of metallization through an intermediate dielectric to possibly contact lower level circuits or metallization.

## BACKGROUND

**[0002]** As will be appreciated by those skilled in the art, most semiconductor devices have several layers of circuits interconnected by vias etched through insulating and/or dielectric materials separating the two levels of circuits and filled with a conductive material such copper, gold, silver or aluminum. To avoid electrical shorts, it is very important that these vias filled with conductive metals do not unintentionally come into contact with other conductive lines and/or devices. Since electrical circuits and devices in an integrated chip are very small, a via that does successfully connect two levels of circuits together, but is misaligned by only a few tenths of microns may cause shorts and render a full wafer of devices useless. As will be appreciated by those skilled in the art, most misaligned vias are the result of a misaligned etching mask. Therefore, it is important that precautions be taken to be sure minor misalignment will not cause shorts. Perhaps the most common way to avoid such destructive electrical shorts is to increase the area that is allocated for the via etch. That is, increase the separation between circuits, or electrical conductive lines, and the location where the via is etched from an upper level to a lower level. This is, of course, a simple and effective solution. Unfortunately, since each of such multi-layer devices will typically include several vias, and since each wafer

includes hundreds of devices, increasing the area for each via is also wasteful and decreases yield.

**[0003]** Therefore, it would be advantageous if misalignment of the etch mask could be avoided so that the area allocated for each via could be reduced.

SUMMARY OF THE INVENTION

**[0004]** These and other problems are generally solved or corrected, and technical advantages are generally achieved, by embodiments of the present invention which provide methods for providing self-aligned features, such as, for example, vias or trenches, on a semiconductor device. The method comprises recessing the top surface of one or more conductors or lines of metallization typically deposited by the Damascene process below the top surface of the surrounding dielectric layer. Recessing the metal may be accomplished by a plasma etch that is selective to the dielectric material or any other suitable process. The recessed conductor or metal lines are then capped by depositing a barrier layer over the top surface of the substrate. The barrier layer may be any suitable material including silicon nitride and silicon carbide and covers the substrate and recessed metal as a substantially constant thickness or conformal coating. Thus, the capping or barrier layer will include a recess directly above the recessed metal lines. According to one embodiment, an intermediate conformal coating or layer of dielectric (ILD) is then deposited over the capping or barrier layer followed by the deposition of a conformal coating of a liner material, such as for example, Tantalum (Ta), Titanium (Ti), Tantalum Nitride (TaN), Titanium Nitride (TiN), Silicon Nitride (SiN) or Silicon Carbide (SiC). However, for certain applications and depending on future processing steps, it may be appropriate to eliminate the depositing of the ILD and deposit the liner material directly over the conformal capping or barrier layer. The layer of liner material is then planarized such that the "high" areas of the conformal liner are removed so that only the low areas remain. However, the "low" areas will also be directly above (aligned with) the metal lines recessed below the top surface of the surrounding dielectric materials. Therefore, by using the remaining areas of the liner layer as a hard mask, vias can be etched through the dielectric layer of the substrate that are

very close to, but not in contact with, the adjacent conductor or line of metallization. Similarly, higher density wiring can be obtained by using this method to etch trenches that extend to a relatively shallow depth in the dielectric. For circuit building purposes, it may be advantageous to create structures with very high capacitance, in which case trenches or similar structures may be formed using the methods of this invention, and which serve the purpose of creating circuit elements with high capacitance. It can therefore be seen that, while via formation is an ideal use of this invention's techniques, one is not limited to forming vias only.

**[0005]** The foregoing has outlined rather broadly the features and technical advantages of the present invention in order that the detailed description of the invention that follows may be better understood. Additional features and advantages of the invention will be described hereinafter which form the subject of the claims of the invention. It should be appreciated by those skilled in the art that the conception and specific embodiment disclosed may be readily utilized as a basis for modifying or designing other structures or processes for carrying out the same purposes of the present invention. It should also be realized by those skilled in the art that such equivalent constructions do not depart from the spirit and scope of the invention as set forth in the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

**[0006]** For a more complete understanding of the present invention, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawing, in which:

**[0007]** FIGs. 1A – 1C illustrate typical prior art steps in providing a metallization level by the Damascene process; and

**[0008]** FIGs. 2A – 2G illustrate the processing steps of the present invention.

## DETAILED DESCRIPTION OF ILLUSTRATIVE EMBODIMENTS

**[0009]** The making and using of the presently preferred embodiments are discussed in detail below. It should be appreciated, however, that the present invention provides many applicable inventive concepts that can be embodied in a wide variety of specific contexts. The specific embodiments discussed are merely illustrative of specific ways to make and use the invention, and do not limit the scope of the invention.

**[0010]** Referring now to the prior art FIG. 1A, there is shown a cross-section of a substrate with conductor or lines of metallization formed in a dielectric. Typically, the lines of metallization will be formed by the Damascene process but could be formed by any other suitable technique. As shown, a substrate 10 is comprised of a first level of dielectric 12 which may include a multiplicity of various types of selected circuits. For example, the connecting pads 14a and 14b may represent connections to lines of metallization or terminals of various circuits such as the bit line of memory cells located in dielectric layer 12. Thus, it should be understood the substrate 10 could represent a single layer of circuits or metallization lines on top of a silicon wafer or, alternatively, the term substrate may be used to represent multiple layers of interconnecting circuits. In any event, there is shown a layer of dielectric material 16 defining a multiplicity of trenches 18a, 18b and 18c etched therein. The sidewalls and bottom of the trenches as well as the top surface of dielectric layer 16 may be covered by a barrier layer or material 20 deposited such as by a CVD (chemical vapor deposition) process to prevent the migration of metallic or metal ions, such as for example, copper ions, into the dielectric. After the barrier layer 20 is deposited, a suitable conductive material 22, such as, for example only, copper, or aluminum, is deposited to fill the trench and cover the top surface of the dielectric layer 16.

**[0011]** The excess copper or conductive material 22 and those portions of the barrier material 20 covering the top surface of the dielectric material 16 are then removed to obtain the strips of metallization 22a, 22b and 22c defined in the lined trenches 18a, 18b and 18c as shown in FIG. 1C. The configuration of FIG. 1C may be achieved, for example, by a two step CMP (chemical-mechanical polishing) process. The first polishing step would use a polishing chemical selective to the barrier layer 20 so as to remove the copper or other metallization down to the barrier layer 20 as shown in FIG. 1B. The second polishing step would then use a chemical selective to the dielectric 16 to remove those portions of the barrier layer or material 20 that are on top of the dielectric 16 as shown in FIG. 1C. It will be appreciated by those skilled in the art that to this point, traditional Damascene processing steps have been used.

**[0012]** Referring now to FIG. 2A and FIG. 2G, there is described an embodiment of the processing steps of the present invention. As shown in FIG. 2A, the surface of the line of metallization or copper 22a, 22b and 22c has been recessed by a process step that is chosen to be selective to the dielectric layer 16. An effective process step for recessing the lines of metallization is to use further CMP with a chemical material that removes the copper or metallization lines 22a, 22b and 22c but is selective to the dielectric layer 16. Other process steps that may be suitable include a metal RIE plasma etch or a wet etch that readily removes the metal, yet is also selective to the dielectric layer 16. No matter the process step selected, the result as shown in FIG. 2A is that the top surface 24 of the lines of metallization (copper) 22a, 22b and 22c is recessed between about 20 nm and 100 nm below the top surface 26 of the dielectric material 16.

**[0013]** After the metal has been recessed, a capping dielectric material or barrier layer 28 such as SiN (Silicon Nitride) or SiC (Silicon Carbide) is deposited as a conformal layer over the

dielectric material 16 and the recessed metal lines of FIG. 2A such that the top surface of the deposited conformal layer of barrier 28 of dielectric material also has a contoured top surface similar to that of the dielectric 16 and recessed metal lines 22a, 22b and 22c as clearly shown in FIG. 2B. That is, the conformal layer defines recesses above, or aligned with, the recessed copper or metal lines 22a, 22b and 22c and the raised areas above the top surface of the dielectric layer 16.

**[0014]** As shown in FIG. 2C, a conformal ILD (Intermediate Layer of Dielectric) 30 may then be deposited over the contoured top surface over the barrier layer 28 such that the top surface of the ILD also defines recesses over or aligned with the metal lines 22a, 22b and 22c. Although it is believed that most devices fabricated according to this invention will typically need or require an ILD layer, for some applications, ILD layer 30 will not be necessary and the step of depositing the ILD layer 30 may be eliminated.

**[0015]** Therefore, referring to FIG. 2D, a liner 32 is deposited on top of the ILD layer 30. However, if the step of depositing ILD layer 30 is eliminated, liner 32 is deposited directly on top of the capping dielectric conformal layer 28. Regardless of whether an ILD layer 30 is included, it is important to understand that the liner 32 will be deposited over a contoured surface having recesses over the metal lines 22a, 22b and 22c and raised portions of the dielectric layer 16 at a substantial constant thickness so that the liner material 32 will also have low or recessed areas over or aligned with the lines of metallization 22a – 22c and high areas over the dielectric material 16. Thus, the liner material 32 conforms with, or is aligned with, the low and high areas of the lines of metallization 22a, 22b and 22c and the dielectric layer 16. Therefore, by planarizing the liner material 32, the remaining low areas 32a, 32b and 32c are aligned with the lines of metallization 22a, 22b and 22c respectively, whereas the high areas of liner material are

removed as shown in FIG. 2E. Thus, it will be appreciated that by selecting a liner material that can be used as a hard mask during an etching step, a self-aligned hard mask is formed that will protect the lines of metallization from a subsequent etching process. According to the present invention, the liner materials believed to be particularly suitable for use as a hard mask include, but are not limited to, Tantalum (Ta), Tantalum Nitride (TaN), Titanium (Ti), Titanium Nitride (TiN), Silicon Nitride (SiN), Silicon Carbide (SiC), or other materials that offer protection during the etch of the underlying dielectric.

**[0016]** Referring now to FIG. 2F, two vias 34a and 34b are illustrated as having been etched through ILD layer 30, capping layer 28 and dielectric layer 16 to contact pads 14a and 14b located on the top surface of the lower dielectric layer 12 and filled with copper or other metallization 35a and 35b. As is clearly illustrated, the self-aligned hard mask portions 32a, 32b and 32c allow the vias 34a and 34b to be precisely located between the lines of metallization without causing an electrical short.

**[0017]** Referring now to FIG. 2G, there is shown an example of a top view of the structure discussed with respect to FIG. 2A through 2F with added strips of resist 36a, 36b and 36c located perpendicular to the strips of hard mask 32a, 32b and 32c, which lie over the lines of metallization 22a, 22b and 22c. The vias 34 are precisely placed in the axis perpendicular to the metal lines through the use of the present invention, and are fixed in the axis parallel to the metal lines through the use of a simplified resist mask (strips 36a, 36b, and 36c) that has much relaxed alignment tolerances because of the use of the present invention.

**[0018]** Previous processes that did not use the self-aligning mask process of the present invention typically required twice as much distance between the two intermediate parallel lines of metallization to minimize effects of misalignment such as electrical shorts between the

conductive via and the adjacent lines of metallization. For example, the circuitry of FIG. 2F requires a conductive via to extend from an upper level, past an intermediate level having lines of metallization, to a lower level.

**[0019]** Although the present invention and its advantages have been described in detail, it should be understood that various changes, substitutions and alterations can be made herein without departing from the spirit and scope of the invention as defined by the appended claims.

**[0020]** Moreover, the scope of the present application is not intended to be limited to the particular embodiments of the process, methods and steps described in the specification. As one of ordinary skill in the art will readily appreciate from the disclosure of the present invention, processes, methods, or steps, presently existing or later to be developed, that perform substantially the same function or achieve substantially the same result as the corresponding embodiments described herein may be utilized according to the present invention. Accordingly, the appended claims are intended to include within their scope such processes, methods, or steps.